In the Claims:

Please amend claims 1-2, 9 and 15-16 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A switching circuit having a first field effect transistor and a second field effect transistor connected in series between an input terminal and a ground terminal, wherein a source [[~~(~~]]of the first transistor is connected to the drain [[~~(4~~]]of the second transistor and a source of the second transistor is connected to the ground terminal[[~~s~~]], the circuit comprising: control means for driving the first and second transistors alternately such that there is a dead time period during which both transistors are off; and means for adjusting the length of the dead time period according to a voltage difference between the drain and the source of the first or second transistor.

2. (Currently Amended) A switching circuit according to claim 1, wherein the first and/or the second transistors are constructed on an integrated circuit die, each of said transistors having respective drain and source regions on said die, further comprising sensing means for sensing the voltag~~lage~~ difference betwe~~1~~8en the drain and the source of the first or second transistors, wherein this sensing means has a first connection, which is directly connected to the source region of the first or second transistor.

3. (Previously presented) A switching circuit according to claim 2, wherein the sensing means has a second connection which is directly connected to the drain region of the first or second transistor.

4. (Previously presented) A switching circuit according to claim 2, wherein the first and/or second connections are Kelvin connections.

5. (Previously presented) A switching circuit according to claim 2, wherein the sensing means senses the voltage difference during the dead time period.

6. (Previously presented)A switching circuit according to claim 1, wherein the adjusting

means adjusts the length of future dead time periods according to the voltage difference during the dead time period.

7. (Previously presented) A switching circuit according to claim 1, wherein the adjusting means adjusts the length of the dead time period according to the length of time that the voltage difference exceeds a threshold voltage.

8. (Previously presented) A switching circuit according to claim 1, wherein the adjusting means adjusts the length of the dead time period according to the magnitude by which the voltage difference exceeds a threshold voltage.

9. (Currently Amended) A switching circuit according to claim 1, wherein the adjusting means adjusts the length of the dead time period such that the length of the dead time period is exponentially dependent on the magnitude by which ~~threshold~~ the voltage difference exceeds ~~the~~ a threshold voltage.

10. (Previously presented) A switching circuit according to claim 1, wherein the adjusting means adjusts the length of the dead time period such that the length of the dead time period is linearly dependent on the length of time for which the voltage difference exceeds a threshold value.

11. (Previously presented) A switching circuit according to claim 1, comprising circuitry to prevent the first transistor from turning on until the second transistor has turned off.

12. (Previously presented) A switching circuit according to claim 1, comprising circuitry to prevent the second transistor from turning on until the first transistor has turned off.

13. (Previously presented) A dc-dc converter circuit comprising the switching circuit of claim 1.

14. (Previously presented) A method of operating a switching circuit having a first field effect transistor sand a second field effect transistor connected in series between an input terminal and a ground terminal, wherein a source of the first transistor (is connected to the drain of the second transistor and a source of the second transistor is connected to the ground terminal, the method comprising: driving the first and second transistors alternately such that there is a dead time period during which both transistors are off; and adjusting the length of the dead time period according to a voltage difference between the drain and the source of the first or second transistor.

15. (Currently Amended) A switching circuit having a first field effect transistor and a second field effect transistor connected in series between an input terminal and a ground terminal, wherein a source of the first transistor is connected to the drain of the second transistor and a source of the second transistor is connected to the ground terminal, the circuit comprising: control means for driving said first and second transistors alternately such that there is a dead time period during which both transistors are off; and means for adjusting the length of the dead time period according to a voltage difference between the drain and the source of the second transistor ~~and the ground terminal~~, wherein the adjusting means adjusts the length of the dead time period according to the length of time for which the voltage difference exceeds a threshold value.

16. (Currently Amended) A switching circuit according to claim 15, wherein the adjusting means adjusts the length of the dead time period according to the magnitude by which the voltage difference exceeds the threshold voltage.

17. (Previously presented) A switching circuit according to claim 15, wherein the adjusting means adjusts the length of the dead time period such that the length of the dead time period is exponentially dependent on the magnitude by which the voltage difference exceeds the threshold voltage.

18. (Previously presented) A switching circuit according to claim 15, wherein the

adjusting means adjusts the length of the dead time period such that the length of the dead time period is linearly dependent on the length of time for which the voltage difference exceeds the threshold value.